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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,445	09/28/2001	Katsuya Anzai	YKI-0077	5332

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EXAMINER
MAGEE, THOMAS J

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,445	ANZAI, KATSUYA	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE f this communication appears n the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1* is/are allowed.

6)☒ Claim(s) *2-6,8,10 and 11* is/are rejected.

7)☒ Claim(s) *7 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2 – 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (US 6,420,200 B1) in view of Arai (US 6,369,507 B1), Takayama et al. (US 5,986,632), and Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publ., Westwood, New Jersey (1993), pp. 357, 386, 389).

3. Regarding Claim 2, Yamazaki et al. disclose a semiconductor device comprising a thin film transistor, in which the transistor and a corresponding element to be driven are electrically connected to each other by a wiring layer (37) (Figures 2 and 14), wherein the element to be driven comprises an emissive layer between a first and second electrode. Yamazaki et al. further disclose a contact hole (Figure 14) formed on an insulation layer (45) above the wiring layer, wherein the wiring layer is connected through the contact hole to the first electrode (51) of the emissive element (47, Figure 2) is formed on top of the insulation layer and covering the contact hole.

Yamazaki et al. do not disclose the presence of a flattening layer, wherein a portion of the hole recess and first electrode regions are covered by the layer. However, the use of flattening (planarization) layers is extremely well known in the art and used routinely for diverse applications on devices (See Wilson et al., p.386, Figures 29 and 31). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the flattening layers of Wilson et al. to partially cover the recess and electrode (partial planarization) in Yamazaki et al. where the emissive element layer and second electrode (49) would be above the first electrode and the flattening layer.
Yamazaki et al. do not explicitly disclose the use of a power supply or driver unit, although it would be obvious that a source of power and a driver circuit would be used for active operation of the system. Arai discloses the use of an organic electro-luminescent device with a switching device and encompassing electrodes (Col. 19, lines 57 – 64). In like fashion, Takayama et al. disclose control and driver circuits for thin film transistors with associated light emissive elements (Col. 7, lines 4 – 32 ; Col. 8, lines 1 – 16). Further, the art is replete with disclosures of power supply and driver/con-troll circuits for electroluminescent display devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Arai and Tokayama et al. with Yamazaki et al. to obtain a power and drive control circuit for controlling the element to be driven at fixed input line points.

4. Regarding Claim 3, Yamazaki et al. disclose a semiconductor device comprising a thin film transistor for controlling power to an element to be driven, which includes an

emissive layer between a first and second electrode (Figure 2), wherein the thin film transistor and element to be driven are directly or indirectly and electrically connected at a contact hole formed on an insulation layer (Figure 2) for separating thin film transistor and at a lower layer than element to be driven. Yamazaki additionally discloses that the first electrode (46) is formed on the insulation layer, covering the contact hole. Yamazaki et al. do not disclose the presence of a flattening layer, wherein a portion of the first electrode recess is covered by the layer. However, the use of flattening (planarization) layers is extremely well known in the art and used routinely for diverse applications on devices (See Wilson et al., p.386, Figures 29 and 31). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the flattening layers of Wilson et al. to partially cover the recess of the electrode (partial planarization) in Yamazaki et al. where the emissive element layer (46) and second electrode (49) would be above the first electrode and the flattening layer.

Yamazaki et al. do not explicitly disclose the use of a power supply or driver unit, although it would be obvious that a source of power and a driver circuit would be used for active operation of the system. Arai discloses the use of an organic electro-luminescent device with a switching device and encompassing electrodes (Col. 19, lines 57 – 64). In like fashion, Takayama et al. disclose control and driver circuits for thin film transistors with associated light emissive elements (Col. 7, lines 4 – 32 ; Col. 8, lines 1 – 16). Further, the art is replete with disclosures of power supply and driver/con-troll circuits for electroluminescent display devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Arai and

Tokayama et al. with Yamazaki et al. to obtain a power and drive control circuit for controlling the element to be driven at fixed input line points.

5. Regarding Claims 4 – 6, Yamazaki et al. disclose (Col. 26, lines 23 – 29) that the element to be driven is an electroluminescent material that is an organic compound.

6. Claims 8, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. in view of Arai, Takayama et al., and Wilson et al.

7. Regarding Claim 8, Yamazaki et al. disclose a semiconductor device comprising a thin film transistor for controlling power to an element to be driven, which includes an emissive layer between a first and second electrode (Figure 2), wherein the thin film transistor and element to be driven are directly or indirectly and electrically connected at a contact hole formed on an insulation layer (Figure 2) for separating thin film transistor and at a lower layer than element to be driven. Yamazaki additionally discloses that the first electrode (46) is formed on the insulation layer, covering the contact hole. Yamazaki et al. do not disclose the presence of a flattening layer, wherein a portion of the first electrode recess is covered by the layer. However, the use of flattening (planarization) layers is extremely well known in the art and used routinely for diverse applications on devices (See Wilson et al., p.386, Figures 29 and 31). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the flattening layers of Wilson et al. to partially cover the recess of the electrode (partial

planarization) in Yamazaki et al. where the emissive element layer (46) and second electrode (49) would be above the first electrode and the flattening layer. Yamazaki et al. do not explicitly disclose the use of a power supply or driver unit, although it would be obvious that a source of power and a driver circuit would be used for active operation of the system. Arai discloses the use of an organic electro-luminescent device with a switching device and encompassing electrodes (Col. 19, lines 57 – 64). In like fashion, Takayama et al. disclose control and driver circuits for thin film transistors with associated light emissive elements (Col. 7, lines 4 – 32 ; Col. 8, lines 1 – 16). Further, the art is replete with disclosures of power supply and driver/con-troll circuits for electroluminescent display devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Arai and Tokayama et al. with Yamazaki et al. to obtain a power and drive control circuit for controlling the element to be driven at fixed input line points.

8. Regarding Claims 10 and 11, as discussed above, Yamazaki et al. do not disclose the presence of flattening layers where partial or complete fill of recesses is done to obtain a partial or near complete planarization. However Wilson et al. disclose (Figure 11) procedures for flattening where the step height reduction (SHR) factor is variable depen-ding on placement from recesses (holes). It would have then been obvious to one of ordinary skill in the art at the time of the invention to use Wilson et al. in Yamazaki et al. to obtain placement of flattening layers either above only the second contact hole to obtain partial flattening or above both holes to obtain continuous coverage for flattening.

Claim Objections

9. Claims 7 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Allowance

10. Claim 1 is allowed. A review of the prior art shows that a semiconductor device that includes an electroluminescent emissive element contained between two electrodes with corresponding power supply and power supply line and thin film transistor connected to an electrode through a wiring layer, wherein the contact position at the transistor is distant from the spatial position of the first electrode and contact point between the wiring layer and first electrode is neither taught or disclosed in the art.

Response to Arguments

11. Arguments of Applicant in regard to Claims have been carefully considered, but are moot in terms of the new ground(s) of rejection. It should be noted that Arai and Takayama are clearly valid as references in terms of the recitations of the instant application. Applicant is also reminded that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; *nor is it that the claimed invention must be expressly suggested in any one or all of the references.* Rather, the test is what the combined teachings of the

references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Hence the combined references of Yamazaki, Arai, and Takayama are clearly valid and the rejections remain.

Conclusions

12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305 5396.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772.**. The fax number for the organization where this application or proceeding is assigned is **(703) 308-7722.**

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
August 19, 2003